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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,534	09/05/2003	Kyong-Mo Bang	TESSERA 3 . 0-328	8773

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,534	BANG ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 2/7/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-45 is/are pending in the application.

4a) Of the above claim(s) 1-8,14-16,22,23,33 and 34 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9-13,17-21,24-32 and 35-45 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/5/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/656534 Attorney's Docket #: TESSERA 3.0-328
Filing Date: 9/5/2003; benefit priority to U.S. Patent Provisional Application 60/408644, filed 9/6/2002

Applicant: Bang et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 9-13, 17-21, 24-32 and 35-45), filed 2/7/05, has been acknowledged. Applicant previously elected the species of figures 1-5.

This application contains claims 1-8, 14-16, 22, 23, 33 and 34 drawn to an invention non-elected without traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9-13, 17-21, 24-32 and 35-45 are rejected under 35 U.S.C. § 102(e) as being anticipated by Degani et al. (U.S. Patent # 6,734,539 B2).

9. Degani et al. (figures 1 to 11) specifically figure 5 **(wherein the assembly (within 71 can be further defined by the elements of figures 3 and 6)** show a semi-finished circuit board assembly comprising: (a) a circuit board **73** having a top surface and contact pads **(shown below 27 in figure 3)** exposed at said top surface; (b) a bottom unit including at least one bottom unit chip **74**, said bottom unit having mounting connections **(shown as 28 in figure 3)** facing downwardly toward said circuit board and top connections facing upwardly away from said circuit board, at least some of said mounting connections being aligned with at least some of said contact pads, at least some of said top connections being unoccupied and available to receive one or more additional microelectronic elements **75,74**.

10. A semi-finished circuit board assembly as claimed in claim 9, Dagani et al show wherein said top connections are adapted **(Note: This use of "adapted" only claims that the top connection can be used to have additional micro electronic elements mounted, it does not claims the structure of microelectronic elements fixed on the unit)** for surface mounting of said one or more additional microelectronic elements **75,74** to said top connections.

11. A semi-finished circuit board assembly as claimed in claim 9, Dagani et al. show wherein at least some of the top connections of said bottom unit overlie at least one said chip in said bottom unit.

12. A semi-finished circuit board assembly as claimed in claim 9, Dagani et al. show wherein said bottom unit includes a substrate **76** incorporating a dielectric element having an upper surface facing upwardly away from said circuit board and a lower surface facing downwardly toward said circuit board, a plurality of mounting pads **(shown as 28 in figure 3)** exposed at the lower surface of said dielectric element and a plurality of top connection pads exposed at the top surface, said at least one bottom unit chip **74** being mounted beneath said lower surface, said mounting connections including said mounting pads **28**, said top connections including said top connection pads (not shown but inherit wit the connection to the terminals of the elements on the top of the substrate).

13. A semi-finished circuit board assembly as claimed in claim 12, Dagani et al. further comprising masses **(shown as 27 in figure 3)** of an electrically conductive bonding material extending between said mounting pads and said contact pads of said circuit board.

17. Degani et al. (figures 1 to 11) specifically figure 5 **(wherein the assembly (within 71 can be further defined by the elements of figure 3)** show a multichip assembly comprising:

(a) a bottom unit including at least one bottom unit semiconductor chip **74**, said bottom unit having downwardly facing mounting pads **(shown as 28 in figure 3)** and upwardly-facing top connection pads (not shown but inherit wit the connection to the terminals of the elements on the top of the substrate);

(b) mounting masses **(shown as 27 in figure 3)** of a fusible electrically conductive bottom bonding material disposed in contact with said mounting pads;

(c) a first packaged semiconductor chip **74,75** having terminals overlying at least some of said top connection pads: and

(d) a top conductive bonding material (not labeled, but shown as the connection between 74,75 and 76) connecting at least some of said top connection pads and at least some of said terminals of said first packaged semiconductor chip,

said top conductive bonding material having lesser height than said mounting masses.

18. An assembly as claimed in claim 17, Dagani et al. show wherein said top conductive bonding material (not labeled, but shown as the connection between 74,75 and 76) is provided in layers less than about 40 microns high and said mounting masses are at least about 100 microns high.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. An assembly as claimed in claim 17, Dagani et al. further comprising a circuit panel **73** having a top surface and contact pads **(shown below 27 in figure 3)** exposed at said top surface, said mounting masses being disposed between said mounting pads and said contact pads of said circuit panel.
20. An assembly as claimed in claim 17, Dagani et al. show wherein said bottom unit includes a substrate **76**, at least a portion of said substrate extending above said bottom unit semiconductor chip, at least some of said top connection pads being disposed on said portion of said substrate.
21. An assembly as claimed in claim 20, Dagani et al. show wherein said substrate is generally planar and includes a central portion (middle of 76) overlying said first bottom unit chip and at least one peripheral portion (border portion of 76) projecting outwardly beyond said first bottom chip, said mounting pads being disposed in said at least one peripheral portion, said mounting masses extending downwardly from said mounting pads.
24. An assembly as claimed in claim 20, Dagani et al. show wherein said bottom unit chip **74** is permanently mounted to said substrate.
25. An assembly as claimed in claim 20, Dagani et al. show wherein said first packaged chip **74,75** includes a die, a package substrate extending beneath such die and terminals on said package substrate, said terminals on said package substrate being bonded to said top connection pads of said bottom unit.
26. An assembly as claimed in claim 19, Dagani et al. show wherein said first packaged chip is a chip-size packaged chip.
27. An assembly as claimed in claim 19, Dagani et al. show wherein said first packaged chip is a standard packaged chip.
28. Degani et al. (figures 1 to 11) specifically figure 5 **(wherein the assembly within 71 can be further defined by the elements of figures 3 and 6)** show an assembly comprising:
(a) a bottom unit including a first bottom unit semiconductor chip **74**, a substrate **76** having a portion extending over said bottom unit semiconductor chip, upwardly-facing

top connection pads (not shown but inherit wit the connection to the terminals of the elements on the top of the substrate) and downwardly facing mounting pads **(shown as 28 in figure 3)** on said substrate, at least some of said top connection pads being disposed in said portion of said substrate, said mounting pads being adapted for connection to contact pads on a circuit board **73**, said bottom unit semiconductor chip being permanently connected to said substrate; and

(b) a first top microelectronic element **74,75** at least partially overlying said portion of said substrate and said bottom unit chip, said top microelectronic element being removably mounted to said substrate and connected to said top connection pads.

29. An assembly as claimed in claim 28, Dagani et al. show wherein said at first top microelectronic element is a packaged semiconductor chip.

30. An assembly as claimed in claim 28, Dagani et al. further comprising a top conductive bonding material (not labeled, but shown as the connection between 74,75 and 76) electrically connecting said top microelectronic element to said top connection pads, said first top microelectronic element being attached to said substrate only by said top conductive bonding material.

31. An assembly as claimed in claim 28, Dagani et al. further comprising a top conductive bonding material (not labeled, but shown as the connection between 74,75 and 76) electrically connecting said top microelectronic element to said top connection pads and attaching said first top microelectronic unit to said substrate at a joint therebetween, said joint being non-underfilled.

32. An assembly as claimed in claim 28, Dagani et al. further comprising an encapsulant **(37 I figure 3)** bonding said bottom unit semiconductor chip to the substrate.

35. An assembly as claimed in claim 28, Dagani et al. show wherein said substrate has electrically-conductive traces (inherit) thereon and said bottom unit chip is electrically connected to said traces by leads integral with said traces.

36. An assembly as claimed in claim 28, Dagani et al. further comprising a circuit panel **73** having contact pads **(shown below 27 in figure 3)** thereon and masses **(27 shown in figure 3)** of an electrically conductive bonding material extending between said mounting pads of said substrate and said contact pads of said circuit panel.

37. Degani et al. (figures 1 to 11) specifically figure 5 **(wherein the assembly (within 71 can be further defined by the elements of figure 3)** show an assembly including:

(a) a bottom unit semiconductor chip **74** having a front surface, a rear surface and edges extending between said surfaces;
(b) a substrate**76** having a central portion extending above said bottom unit semiconductor chip, said bottom unit semiconductor chip being mounted to said central portion of said substrate with a surface of the chip facing upwardly toward the substrate, said substrate also having one or more peripheral portions projecting outwardly beyond the edges of the chip;
(c) first and second top microelectronic elements **74,75** disposed above said substrate, at least one of said top microelectronic elements extending over said central portion and at least one of said top microelectronic elements extending over said peripheral portion; and
(d) mounting terminals **(shown as 28 in figure 3)** on said substrate electrically connected to at least one of said chips and adapted for mounting said substrate to a circuit board **73**.
38. An assembly as claimed in claim 37, Dagani et al. show wherein said bottom unit semiconductor chip has greater surface area than either of said first and second top microelectronic elements alone.
39. An assembly as claimed in claim 37, Dagani et al. show wherein said bottom unit semiconductor chip has a surface area less than the aggregate surface area of said first and second top microelectronic elements.
40. An assembly as claimed in claim 37, Dagani et al. show wherein said at least one peripheral portion includes first and second peripheral portions projecting beyond opposite edges of said bottom unit semiconductor chip, and wherein said first top microelectronic element overlies said first peripheral portion and part of said central portion and said second top microelectronic element overlies said second peripheral portion and another part of said central portion.
41. An assembly as claimed in claim 40, Dagani et al. show wherein said mounting terminals include mounting pads **(28 in figure 3)** disposed in said first and second peripheral portions.
42. An assembly as claimed in claim 41, Dagani et al. show wherein at said first and second top microelectronic elements overlie at least some of said mounting pads disposed in said first and second peripheral portions.

43. An assembly as claimed in claim 37, Dagani et al. show wherein said bottom unit semiconductor chip is permanently connected to said substrate and said top microelectronic elements are removably connected to said substrate.
44. An assembly as claimed in claim 37, Dagani et al. show wherein said first and second top microelectronic elements are packaged semiconductor chips.
45. An assembly as claimed in claim 37, Dagani et al. further comprising a circuit panel **73** having contact pads **(shown below 27 in figure 3)** thereon and masses **(27 shown in figure 3)** of an electrically conductive bonding material extending between said mounting pads of said substrate and said contact pads of said circuit panel.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,723,700,701,758,725,728,778,779,780, 784,786,737,734,738,692,693 361/783,760,767,768,770,771,803	4/29/05
Other Documentation: foreign patents and literature in 257/686,685,777,723,700,701,758,725,728,778,779,780, 784,786,737,734,738,692,693 361/783,760,767,768,770,771,803	4/29/05
Electronic data base(s): U.S. Patents EAST	4/29/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/11/05